REMARKS

Claims 1-16 are pending in the present application, claims 5-13 having been selected for examination and claims 1-4 and 14-15 having been withdrawn pursuant to a restriction requirement. The Office Action and cited references have been considered. Favorable reconsideration is respectfully requested.

The Examiner has rejected claims 5, 6, 9, 12 and 13 under 35 U.S.C. §102(b) as being anticipated by Duboc *et al.* (US 6,415,116). The Examiner has further rejected claims 7 and 8 under 35 U.S.C. §103(a) as being obvious over Duboc *et al.* in view of Gupte et al (US 5,903,475), and claims 10-11 as being obvious over Duboc et al in view of Gupte *et al.* and further in view of Hekmatpour(US 2002/0156929).

The following comments will help to clarify what Applicant believes are the distinguishing features of the invention as defined by the revised claims, over Duboc *et al.*

Duboc *et al.* relates to a design tool for a DSP. Thus, by way of example, reference is made to the abstract, which recites:

> An apparatus, program product and method are provided for use in automatic design of a custom **DSP integrated circuit** from a preexisting **DSP** code block and one or more

> additional circuit blocks interfaced with the **DSP** core block. (emphasis added)

Unlike the current invention, which deals with ASIC (Application Specific Integrated Circuit) design, Duboc *et al* describes DSP (Digital Signal Processing) design tools. In light of the foregoing difference, the applicant maintains that independent claim 5, and the claims appended thereto, are novel over Duboc *et al*.

Furthermore, Gupte *et al*. describes the use of script files for automating synthesis as is seen in Col. 7, lines 15-17:

> The synthesis scripts are designed according to a **synthesis** strategy designed for the **synthesis tool**. In one embodiment the **synthesis tool** is Synopsys. (emphasis added)

This is different from the claims of the current invention, which specifically exclude synthesis.

In addition, Hekmatpour describes the following in the field of the invention:

> The present invention relates in general to **system-on-chip** (**SoC**) and in particular to the design of **SoCs**... (emphasis added)

Unlike the current invention, which deals with ASIC design, Hekmatpour describes System-on-Chip design **collaboration** tools. Moreover, there is no motivation in

Hekmatpour to combine the teachings of Duboc *et al* and Gupte *et al*. Such a combination, even if possible, would not result in the invention as claimed. It is respectfully submitted that any suggestion that the present claims are obvious over such a combination is not supported by any of the cited references taken either singly or in combination and amounts to mere hindsight.

Support for the amendments is found in the present application, e.g. on page 3, lines 26-27:

> It is therefore an object of the invention to provide a method and system that enhances the computerized **ASIC design** process. (emphasis added)

Furthermore, page 5, lines 3-4, for example, recites:

> The invention also supports computerized insertion of scan chains into the ASIC in the **DFT (Design For Test)** process. … (emphasis added)

DFT is further recited, e.g., with reference to Fig. 4.

Page 5, lines 9-15, e.g., recites:

> The produced netlist should be compared against the initial HDL developed in the ASIC design process, to check the agreement of both. This comparison is referred to as verification, and it is also composed of two stages: dynamic verification (real world

> signal emulation to the as yet virtual ASIC) and **static verification** (comparing the netlist with the HDL code to check their formal agreement). Dynamic verification is also known in the art as simulation, while static verification is referred to as formal verification. … (emphasis added)

Page 5, lines 25-30, for example, recites:

> … based on the timing constraints specified by the budget stage, on the layout constraints generated by the ASIC designer and on the netlist generated by the synthesis stage, the **physical compile** performs a layout based synthesis, i.e. it locates speeded-up and slowed-down elements on the ASIC while moving and switching between elements already located on it by the synthesis stage in order to find vacant locations for all. (emphasis added)

According to a different example, physical compile is illustrated also in Fig. 4.

Page 6, lines 1-5, for example, recites:

> Testing the timing of an ASIC that passed the layout and/or the physical compile stages combines formal and static analysis in a stage referred to as **physical STA**. The physical STA tools perform timing analysis, using the output of the layout as their input, the output of the layout including Standard Delay Format (SDF) files which represents the actual delays on the physically placed netlist. … (emphasis added)

Physical STA is also illustrated, e.g., in Fig. 5.

ECO (Electrical Change Order) is mentioned, for example, in page 6, lines 14-15:

> In the **ECO** process specific elements and connections can be inserted or removed by manually to the netlist. … (emphasis added)

ECO further appears, for example, in Fig. 6.

Turning now to the newly introduced Claim 16, support is found, e.g., in page 8, lines 2-7:

> the invention provides automatic integration with version control tools, automatically tracking modifications to files developed in the design process. Using version control tools can help also in organizing the ASIC integration process, as versions can be properly marked. Automatically integrating version control tools into the ASIC design process encourages and simplifies their usage.

Claims 5, 9 and 12 were rejected under 35 U.S.C. § 112, second paragraph. Applicant has amended claims 5 and 12 to overcome the rejection. However, relating to the Examiner's comments to Claim 9, the Applicant respectfully points out that e.g., according to page 11, lines 20-21 of the application:

> The automatically generated scripts are formed, based on a pre-prepared template scripts. ...

See also, page 8, lines 19-22. According to, e.g., page 7, lines 21-22:

> Command files, i.e. scripts, relating to each selector are stored in the memory of the synthesis manager, to be automatically executed when the selector is selected.

Further, Applicant notes that page 7, lines 15-18 of the present application, cited by the Examiner states:

> Fig. 1 Illustrates an exemplary interface supporting ASIC synthesis manager according to one embodiment of the invention. The interface supports the activation of each synthesis stage, and the display of each stage's results and statistics, by selecting any selector, i.e. button, from the graphical interface.

This portion says nothing about the selectors being part of the templates; it does not mention templates at all.

Applicant maintains that claim 9 correctly recites that pre-prepared templates are parts of the selected selectors and not the opposite. Withdrawal of this rejection is respectfully requested.

Applicant notes that the PTOL-326 form indicates that the drawings filed on March 2002 were objected to by the Examiner. The Office Action mailed on January 13, 2005, did not include any indication of the objections, which are raised by the Examiner. Applicant notes that substitute drawings were filed on April 19, 2002 in reply to the notice to file corrected application papers. If this objection is maintained, the Examiner is requested to provide a detailed

description of the objections so that the appropriate corrections can be made.

In view of the above amendments and remarks, Applicant respectfully requests reconsideration and withdrawal of the outstanding rejections of record. Applicant submits that the application is in condition for allowance and early notice to this effect is most earnestly solicited.

If the Examiner has any questions she is invited to contact the undersigned at 202-628-5197.

Respectfully submitted,

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